IN THE SPECIFICATION:

Please replace paragraph [0026] with the following amended paragraph:

[0026] Figure 1A shows a cross section through the dynamic memory cell before formation of the bit-line contact, on which cell structures have been produced during preceding process steps. The memory cell comprises a trench capacitor 20 and a select transistor 30, which is preferably produced with the aid of planar technology. The select transistor 30 comprises two n-doped diffusion regions 31 in a p-doped semiconductor substrate 10, which define the source/drain electrodes, and a highly n-doped region 32 above a channel 33 between the two n-doped diffusion regions 31, which region 32 is located within an insulator layer 40 and forms the gate electrode. The trench capacitor 20 is filled with a highly n-doped material 23 which forms the inner capacitor electrode. This electrode is separated from a likewise highly n-doped region 11 in the semiconductor substrate 10, which forms the outer electrode of the trench capacitor, by a thin film 21 with a high dielectric constant ε_r.

Please replace paragraph [0027] with the following amended paragraph:

[0027] To form an electrically conductive connection to one of the ~~highly~~ n-doped diffusion regions 31 of the select transistor 30, the outer electrode 11 of the trench capacitor 20 has an overlap with one of the n-doped diffusion regions 31 (i.e., the source/drain electrode of ~~31 of~~ the select transistor 30).